WHAT IS CLAIMED IS:

1. A semiconductor apparatus including a MOS-type device, comprising:

a first switch for supplying a gate current during a turn-on operation for turning on the gate of said MOS-type device;

a second switch for discharging a gate capacitance during a turn-off operation for turning off the gate of said MOS-type device;

a third switch for increasing said gate current;

first timer means for turning on said third switch in conjunction with the turn-on of said first switch, and then turning off said third switch after a first predetermined time from said turn-on of said third switch;

a fourth switch for increasing the discharge current during said gate turn-off operation; and

second timer means for turning on said fourth switch in conjunction with the turn-on of said second switch, and then turning off said fourth switch after a second predetermined time from said turn-on of said fourth switch.

2. The semiconductor apparatus as defined in claim 1, which includes:

a second gate turn-on circuit other than a first gate turn-on circuit having said first and third switches; and

means for detecting a collector current of said MOS-type device,

wherein when said detected collector current is less than a predetermined value, only said first gate turn-on circuit is activated to provide the gate current at a first amount, and

when said detected collector current is equal to or greater than said

predetermined value, both said first and second gate turn-on circuits are activated to provide the gate current at a second amount greater than said first amount.

3. The semiconductor apparatus as defined in claim 2, wherein when the detected collector current of said MOS-type device turned on according to a first turn-on operation is equal to or greater than said predetermined value, said second gate turn-on circuit is activated in a second turn-on operation subsequent to said first turn-on operation.

4. The semiconductor apparatus as defined in claim 1, wherein said first predetermined time is set at a value allowing said MOS-type device to be turned on after said first and third switches are turned on, and said second predetermined time is set at a value allowing said MOS-type device to be turned off after said second and fourth switches are turned on.